Modeling MESFET's for Intermodulation Analysis in RF Switches

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***Abstract*— This paper describes a new model for a resistive GaAs MESFET and its application to calculations of intermodulation distortion in switches. The model uses an expression for the I/V characteristics of the device whose parameters are fit to the static I/V and its derivatives. This new model provides a reliable means of describing the nonlinear distortion generated by a MESFET switch.**

I. Introduction

In recent years, the availability of general purpose harmonic-balance and Volterra-series simulators has generated a need for accurate nonlinear models of GaAs MESFET's, and many FET models have been proposed. Most of these models are not valid for passive FET's [1], [2], and missing from those that do apply is an assessment of the properties of a model that are necessary for the accurate calculation of intermodulation distortion [3], [4]. Models are usually designed to reproduce the FET's static current-voltage (I/V) and charge-voltage (Q/V) characteristics when, in fact, the derivatives of those characteristics are dominant in determining intermodulation levels. We propose a new model for the MESFET gate I/V characteristic (the dominant nonlinearity in most FET's) that is accurate through at least the third derivative. Although utilized in the distortion analysis of an RF switch, this model is accurate over a large range of bias voltages and is applicable to all passive FET's operating in applications such as phase shifters, attenuators, and resistive mixers.

II. Modeling GaAs MESFET's

It was shown recently that modeling nth-order intermodulation distortion in mixers requires that the device's model reproduce accurately the first n derivatives of its I/V and Q/V characteristics over its entire voltage or current range of operation [1]. In a passive FET, the channel is used as a gate-voltage-controlled resistor, and its I/V characteristic is necessarily a function of two voltages, the gate-to-source and drain-to-source voltages. In this case it is necessary that the model reproduce not only the derivatives of the drain current with respect to these control voltages, but also the partial derivatives of the current with respect to both voltages. The fundamental difficulty lies in accurately modeling all of the terms in a two-dimensional Taylor-series expansion of the drain current.

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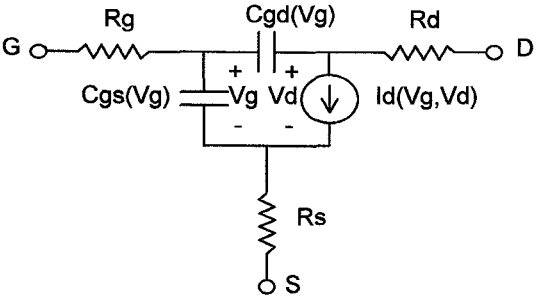

Fig. 1. Equivalent circuit of a GaAs MESFET operated at zero drain voltage.

Fortunately, for FET switches, the Taylor-series expansion can be simplified. The nonlinear conductance of the channel is controlled by the voltage at the gate, and the RF signal is applied to this gate-voltage-dependent conductance. Thus, in this configuration, the small-signal gate voltage v_g is small and there is no dc bias at the drain, $V_{d_o} = 0$. The derivatives, and therefore the Taylor-series expansion coefficients, are functions of the large-signal (dc) gate voltage and the constant drain voltage. The small-signal expression of the drain current (to third degree) becomes:

$$i_d(V_g, V_{d_0}) = i_d(V_g, 0) = g_1(V_g, 0)v_d + g_2(V_g, 0)v_d^2 + g_3(V_g, 0)v_d^3$$

where

$$g_n(V_g, 0) = \frac{1}{n!}\frac{\partial^n I_d}{\partial V_d^n}$$

i_d and v_d represent incremental current and voltage, and the partial derivatives are evaluated at the control voltages, the large-signal (usually dc) voltages V_{g_0} and V_{d_0}.

Fig. 1 shows the equivalent circuit of a MESFET without drain bias voltage. The distributed gate-to-channel capacitance is represented as two voltage-controlled capacitances, $C_{\rm gs}(V_g)$ and $C_{\rm gd}(V_g)$. R_g is the gate resistance, and R_d and R_s are the parasitic drain and source resistances. The drain current is $I_d(V_g, V_d)$, a function of both the gate and drain voltages.

Measuring the I/V characteristic at dc and calculating the derivatives numerically is usually impractical because the FET's nonlinearity is very weak, and is often lost within measurement tolerances. Instead, we measure the derivatives indirectly by applying a low-frequency RF signal to the FET channel, in a manner similar to that of [1] and [5]. The Taylor-series expansion coefficients are then extracted from measure-

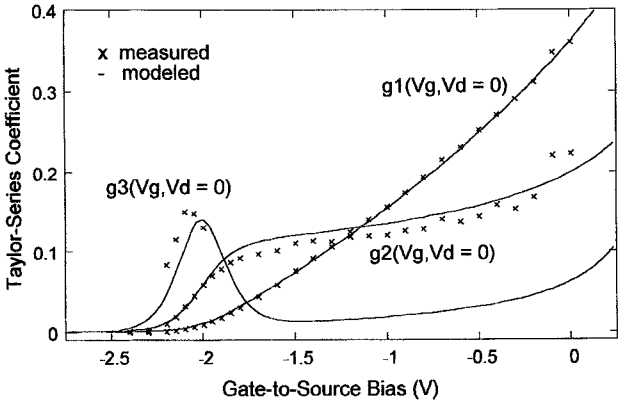

Fig. 2. Measured (x) and modeled ($-$) Taylor-series expansion coefficients of the I/V characteristic of an NEC NE72084 MESFET. The device parameters are $I1$ =0.49 A, V_p =2.81 V, ϕ =0.8 V, $R_d = R_s$ =0.55 Ω, α =4, β =1.5, γ =0.01, $\delta = -0.0031$ and ε =0.0026.

ments of the harmonic output power by means of Volterra-series analysis and the method of nonlinear currents [6].

We use an I/V expression for the passive FET that accurately reproduces the measured static I/V and its derivatives. Because a FET in a switch operates at low drain voltages, the electron velocity-field characteristic is nearly linear and the channel may be modeled by Shockley's theory [7]. Unfortunately, the Shockley model is not accurate near pinchoff, so we use an empirical correction term. By multiplying a modified Shockley drain current by this correction term, the derivatives can be fit to the measured data. The correction term is

$$F(V_g, V_d) = \frac{1}{2}\left[1 + \frac{2}{\pi}\text{atan} \times [\alpha(V_g - V_d + V_p - \phi)]\right]$$

where V_p, the pinch-off voltage, and ϕ, the junction potential, are defined as a positive quantities and the α term is used to control the rate of channel depletion with respect to bias.

The I/V expression becomes

$$I_d(V_g, V_d) = I1\left[\frac{3\beta V_d}{V_p} - 2\left[\left[\frac{\beta V_d - V_g + \phi}{V_p}\right]^{\frac{3}{2}} - \left[\frac{-V_g + \phi}{V_p}\right]^{\frac{3}{2}}\right]\right] F(V_g, V_d) + \gamma V_d + \delta V_d^2 + \varepsilon V_d^3$$

The final terms in the expression have been introduced to ensure that the conductances $g_1(V_g, V_{d_0}$ =0), $g_2(V_g, V_{d_0}$ =0), and $g_3(V_g, V_{d_0}$ =0) approach zero at the pinch-off voltage.

Fig. 2 compares the measured and modeled Taylor-series expansion coefficients of the I/V characteristic of an NEC NE72084 MESFET. In order to obtain an accurate representation of the I/V expression and all its derivatives, we fit this model to the measured $I_d(V_g, V_d)$ and its derivatives by adjusting the parameters of the device ($I1$ =0.49 A, V_p =2.81 V, ϕ =0.8 V, $R_d = R_s$ = 0.55 Ω, α =4, β =1.5, γ =0.01, $\delta = -0.0031$, and ε =0.0026). Note that the sensitivity of the test setup limits the measurable power levels and thus the measurable data points for g_3. If we were to make a similar plot

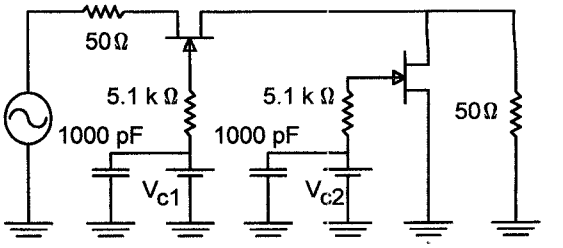

Fig. 3. GaAs FET RF switch circuit.

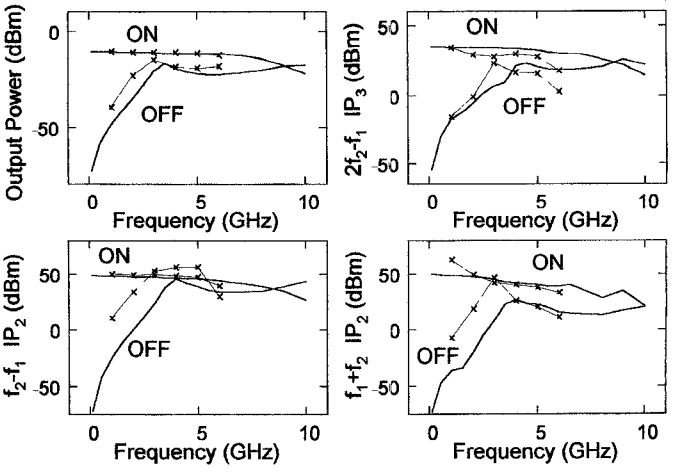

Fig. 4. Measured (x) and modeled ($-$) output power and intercept points (**IP**) for the "ON" state (V_{c1} =0 V and $V_{c2} = -2.6$ V) and the "OFF" state ($V_{c1} = -2.6$ V and V_{c2} =0 V) of the RF switch. The input level is -10 dBm per tone.

using the model described in [4], both g_2 and g_3 would be zero for all gate biases. Because the drain is unbiased, the gate-to-channel capacitance is divided approximately equally between the gate-to-source and gate-to-drain capacitances. These are modeled as ideal Schottky-barrier capacitances, with uniform epitaxial doping:

$$C_{gs}(V_g) = C_{gd}(V_g) = \frac{C_{g_o}}{\sqrt{1 - \frac{V_g}{\phi}}}$$

III. Results

We installed this model into the general-purpose harmonic-balance program Microwave Design System (MDS) to simulate the performance of the RF switch circuit shown in Fig. 3. The switch was realized on microstrip substrate (RT Duroid 5870) utilizing the layout option available on MDS. With an input level of -10 dBm per tone, output signals were measured using a method similar to that described in [6]. The measurements were compared to the simulated results for the second- and third-order distortion components located at $f_2 - f_1$, $f_1 + f_2$, $2f_1 - f_2$, and $2f_2 - f_1$, and the results are shown in Fig. 4. The control voltages were: V_{c1} =0 V, $V_{c2} = -2.6$ V for the "ON" state and $V_{c1} = -2.6$ V, V_{c2} =0 V for the "OFF" state. It was assumed that the parameters of the two devices were identical with the exception of the measured pinch-off voltages.

Data were obtained for a variety of bias voltages, and as expected by the model, the distortion depended directly on

the dc bias levels. The model appears to effectively predict distortion, although there is a noticeable discrepancy with regard to frequency that is founded in the linear characterization of the test circuit and passed on to all data points via the intercept point (IP) calculation. There are also errors, as one might expect, at high frequencies and high-order distortion. The errors suggest that it may be necessary to use a new capacitance model, especially near pinchoff, where the assumption of uniform doping loses validity. The worst errors are at sum frequencies, where they are probably affected by limited accuracy of the linear parts of the FET model in addition to the characterization of the test circuit. Note that a comparison of this model to Shockley and Materka [8] has been performed, but it is not presented here because these models do not account for pinchoff and provide inaccurate linear results that further degrade the accuracy of their predicted intercept points.

IV. Conclusion

A new model for calculating intermodulation distortion in GaAs MESFET switches has been developed. By accurately expressing the I/V characteristics of the FET device as well as the derivatives of those characteristics, this model predicts distortion and is the first of its kind for passive devices. It is accurate over a large range of bias voltages and is applicable to all FET's operating in the passive mode, such as phase shifters, attenuators, and resistive mixers.

Acknowledgment

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